COSC 3327

Dr. Tim McGuire

**EXAM #1**

*Sample*

1. Draw the gate diagram symbols for
   1. a NOT gate
   2. an XNOR gate
   3. a NAND gate
2. Draw the transistor diagram for an inverter (NOT gate.)
3. Define
   1. combinational logic
      1. Combinational logic is: outputs are dependent only on the current inputs.
      2. Ex:
         1. Adder
         2. multiplexor
   2. sequential logic
      1. Sequential logic is: the output is dependent on the current inputs and past inputs
         1. Ex.
            1. Vending machine change. Gumball machine
            2. Memory in a computer
            3. RS Flip-flop

Uses nor gates

Hooked up in a feedback circuit.

S – qbar

R – q

1. Consider the Boolean logic expression: **F = (AB + C) + (B AC̅**). Draw a circuit diagram based directly on the formula using AND, OR, XOR, and NOT gates.
2. For the above Boolean expression, construct a K-map, minimize the circuit, and give the sum-of-products form of the minimized expression.
3. Show that the following gates can be implemented entirely using only 2-input NAND gates:
   1. NOT
   2. 2-input OR
   3. 2-input AND
4. A 1-bit half adder has the following truth table. Construct an appropriate circuit diagram:  
     
    **A B S C** 0 0 0 0  
    0 1 1 0  
    1 0 1 0  
    1 1 0 1
5. Draw the gate-level logic diagram for a 4-to-1 MUX, a circuit in which one of four data input lines are connected to its single output, depending on the state of its two control lines.
6. You have been constructing a circuit and discover that you need one additional AND gate, but all you have is a chip with 2-to-1 MUXs. Show how to connect a 2-to-1 MUX to serve as an AND gate. (Assume you have access to Vcc and Ground, in addition to your logic inputs.)  
     
    D0  
    F  
      
    D1 A
7. Draw the gate-level logic diagram for an RS flip-flop. Label all inputs and outputs correctly (**R**, **S, Q**, **and Q̅**.)
8. Draw the logic gate diagram for a clocked D flip-flop. You may use a block diagram for an RS flip-flop in your solution.
9. Convert **11111101** to decimal treating it as: **Do in sleep**
   1. unsigned
   2. 1’s complement
   3. 2’s complement
   4. sign-magnitude
10. The first 32 bits of every Java class file are **CAFE BABEh**. Convert this to 32-bit binary, then to octal.
11. Convert **429** (base 9) to base 3:
12. Convert the following decimal numbers to IEEE single-precision floating-point numbers. Report the results as hexadecimal numbers. (You need not extend the calculation of the mantissa value beyond its most significant 8 bits.)
    1. 8.25
    2. –4.5
       1. -4.510 = -100 .12
13. Convert the following IEEE single-precision floating-point numbers to their base-10 values.
    1. **3F60 0000h**
    2. **BF90** **0000h**
14. What it the smallest normalized positive IEEE single-precision floating-point number can you represent? Explain.
    1. The smallest stored value = 1; so you’d have to subtract the bias of 126. So the fraction is 1.0 ………. ?
15. Translate the following into MIPS Assembly language. A = a-b+c-d. assume they are in regs $s1-$s4
16. The MIPS processor has no PUSH or POP opcodes. Explain how processor performs the equivalent operations.
    1. ?????
17. Moore's Law state that computing power doubles every 18 months for the same price. As of October 2009, a computer scientist at NASA has just built a cluster of 128 “typical” desktop machines that can solve a mathematical problem in 16 hours. On what date will our scientist be able to build a cluster of 16 “typical” desktop machines that will solve the same problem in 4 hours?
    1. Firstly, every machine has to be 32x faster
    2. So 32 = 25
    3. 5 “doublings”
    4. 5x 1.5 years – 7.5 years
       1. therefore April of 2017 he should expect to do it.
18. We wish to compare the CPU performance of two computers, A and B, when executing program P. We know that the processors in A and B both implement the same instruction set architecture. We can determine the following information for A and B:

(1) The Instruction Count (number of instructions executed) for Program P

(2) The Clocks Per Instruction (CPI) for Program P

(3) The Clock Rate

Which of these must be determined for both A and B in order to make a valid comparison?

1. CPI and clock rate can be different.
3. A 1.6GHZ machine takes 8 clock cycles for every instruction. You wish to make sure that your function completes in less than 2 microseconds. To how many instructions should you limit your function?
   1. CPI = 8;
   2. # instructions = (using dimensional analysis)
4. Consider a special floating-point representation that is the same as IEEE single and double precision (with the largest exponent value representing infinity and NaN), except that the **exponent** field is 3 bits and the **significand** field is 4 bits, for a total of 8 bits (once we include the sign bit). With this representation:
   1. What is the value in base 10 of the largest representable positive number? (infinity and NaN are not numbers.)
   2. What is the value in base 10 of the smallest representable positive number (not zero)? (infinity and NaN are not numbers. You may represent the result as a fraction rather than as a decimal.)
   3. How many numbers total can be represented? (infinity and NaN are not numbers.) 193 numbers